Ain Shams University

Faculty of Engineering

CHEP- CESS

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Electronic Design Automation

CSE 215

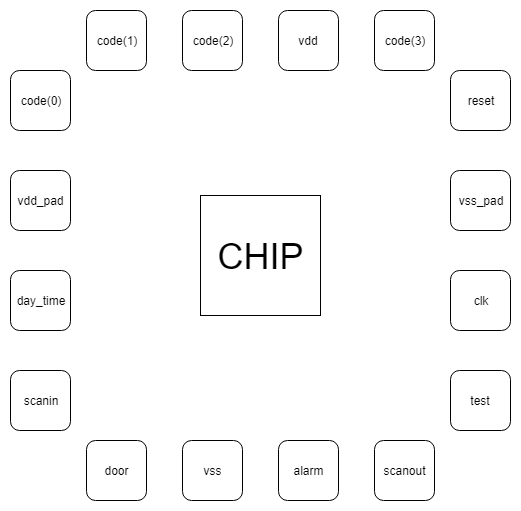
Digital Access Control Finite State Machine Project 3

Introduction

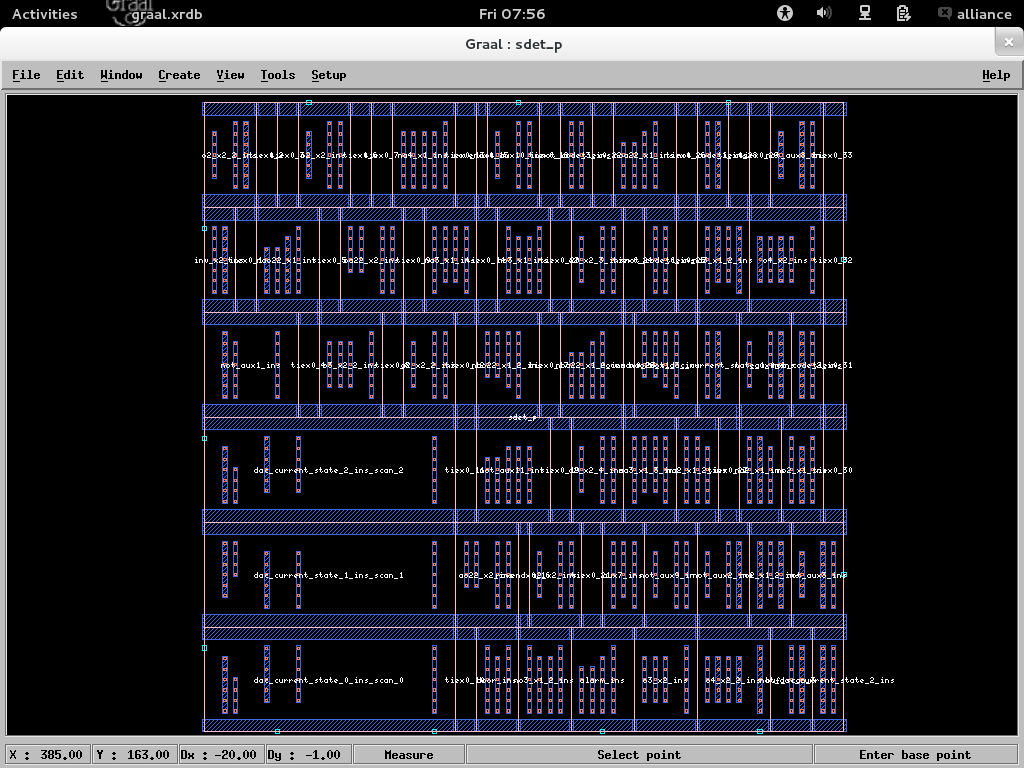
The purpose of this document is to illustrate the usage of Alliance tools to perform placement and routing to the digital access control finite state machine created and synthesized in project one and project two respectively.

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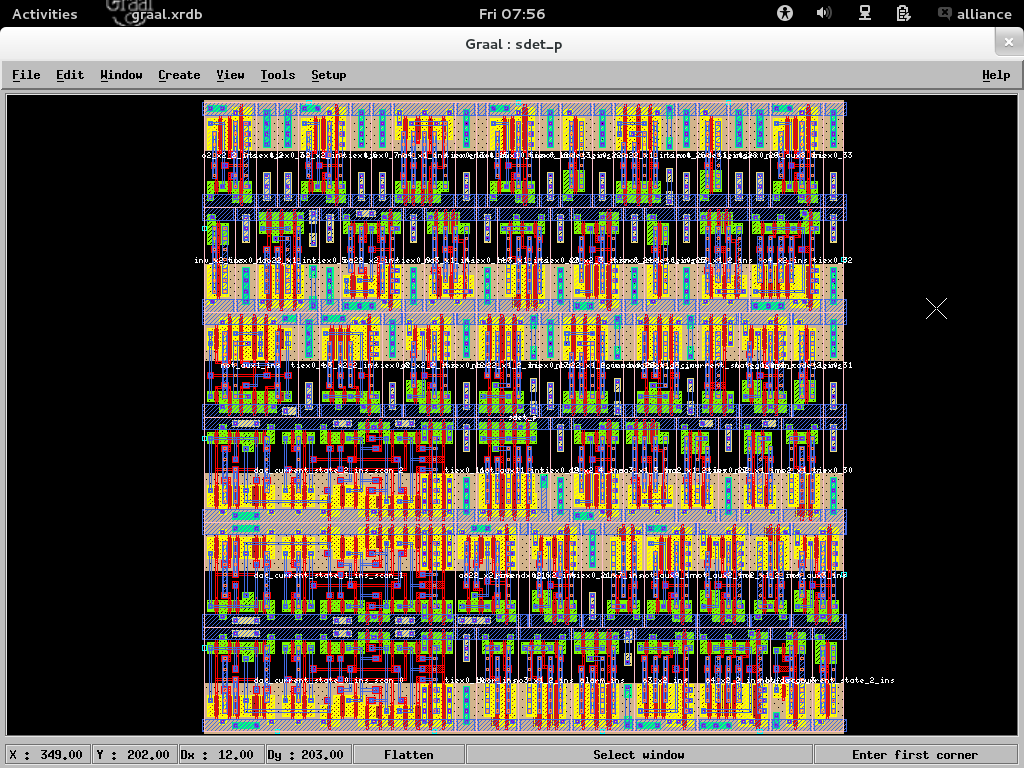
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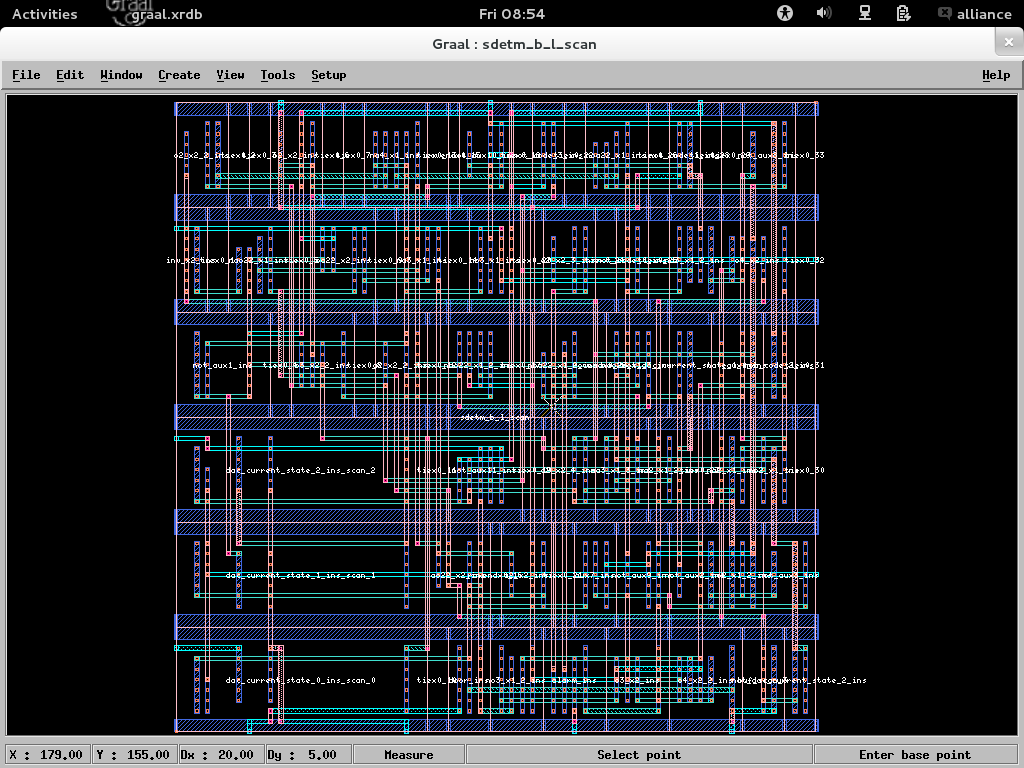
1. OCP Output Layout View using Graal



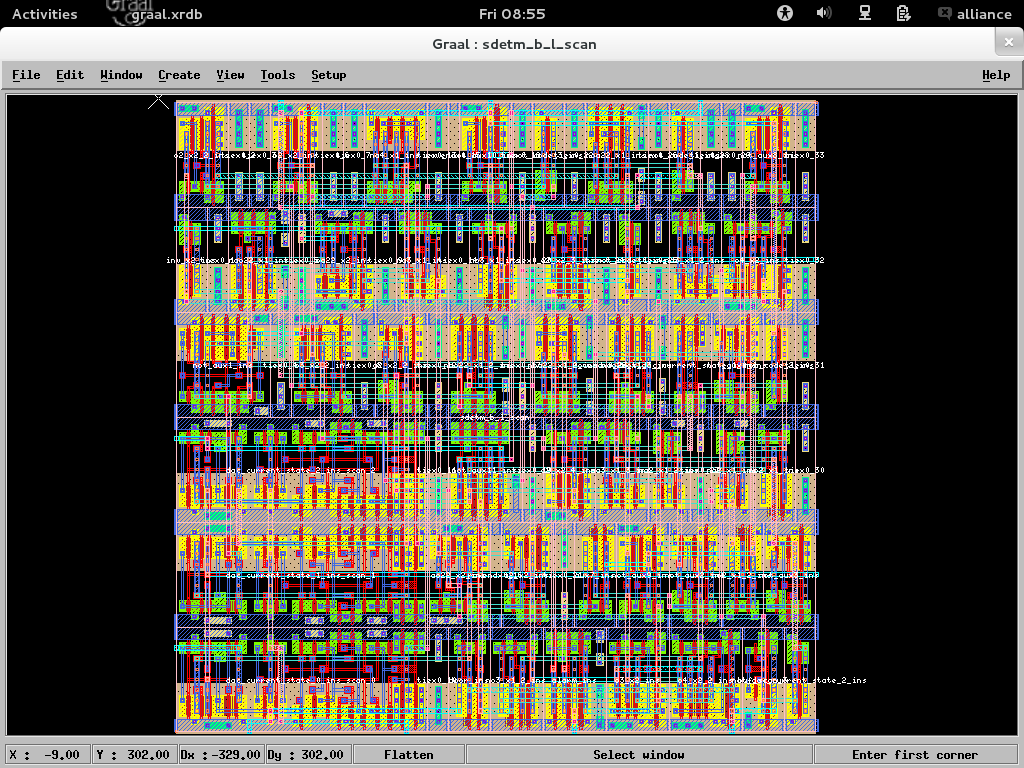
1. OCP Output Layout Flattened View using Dreal



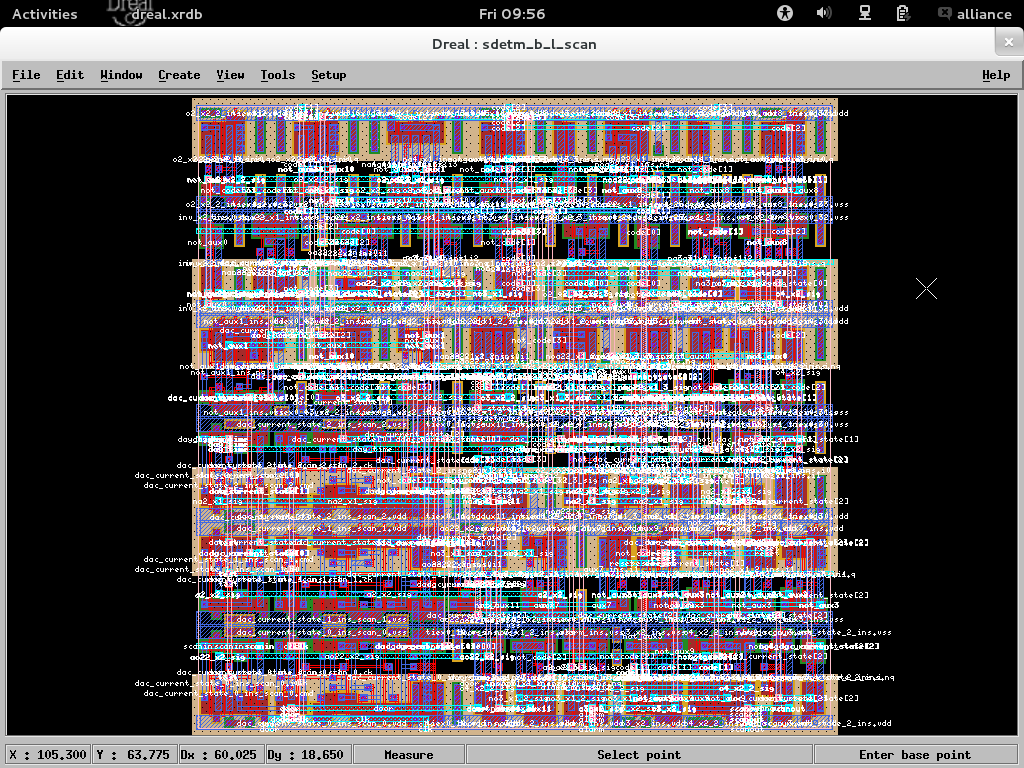
1. Nero Output Layout View using Graal



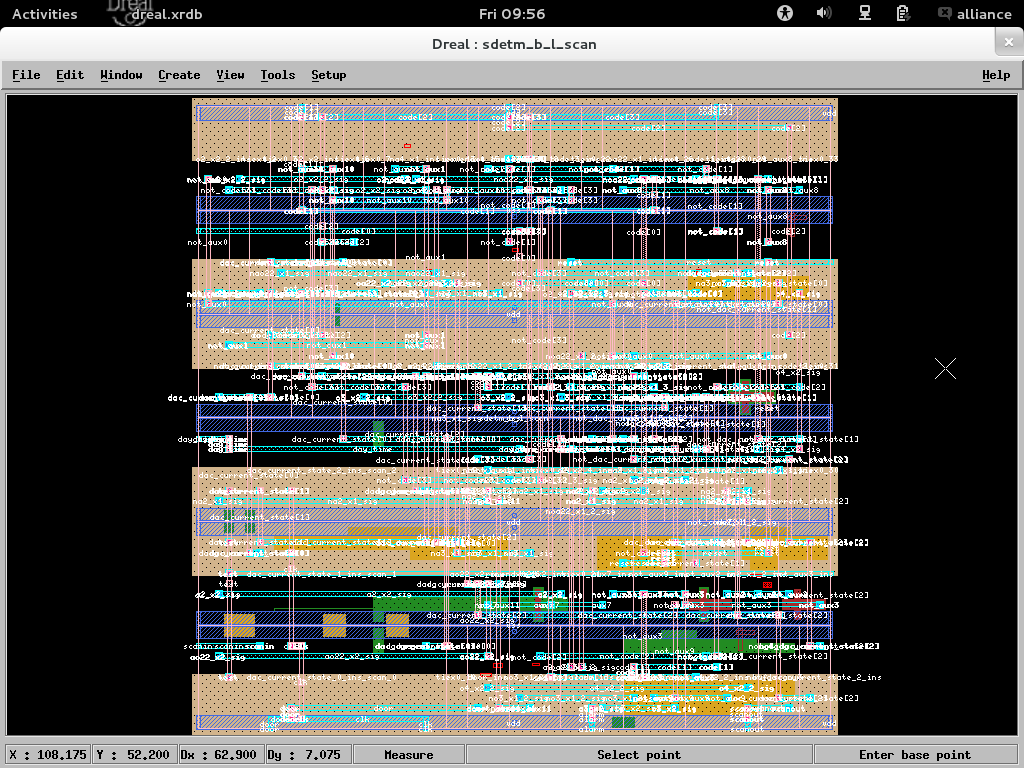
1. Nero Output Layout Flattened View using Graal



1. S2R Output Layout Flattened View using Dreal



1. S2R Output Layout View using Dreal



1. Appendix

# Makefile

sdetm\_p.ap\_ocp : sdet.ioc sdetm\_b\_l\_scan.vst

    MBK\_IN\_LO=vst; export MBK\_IN\_LO; \

    MBK\_OUT\_PH=ap; export MBK\_OUT\_PH; \

    ocp -v -ring -ioc sdet sdetm\_b\_l\_scan sdet\_p > ocp.out

sdetm\_b\_l\_scan.ap\_nero : sdet\_p.ap sdetm\_b\_l\_scan.vst

    nero -V -p sdet\_p sdetm\_b\_l\_scan sdetm\_b\_l\_scan > nero.out

%.al\_cougar\_lvx : %.ap

    MBK\_OUT\_LO=al; export MBK\_OUT\_LO; \

    RDS\_TECHNO\_NAME=./techno/techno-035.rds; \

    export RDS\_TECHNO\_NAME; \

    cougar -v $\* > cougar\_$\*.out

    lvx vst al $\* $\* -f > lvx\_$\*.out

druc\_core : sdetm\_b\_l\_scan.ap

    RDS\_TECHNO\_NAME=./techno/techno-symb.rds; \

    export RDS\_TECHNO\_NAME; \

    druc sdetm\_b\_l\_scan > druc\_core.out

sdet\_chip.cif : sdetm\_b\_l\_scan.ap

    RDS\_TECHNO\_NAME=./techno/techno-035.rds; \

    export RDS\_TECHNO\_NAME; \

    RDS\_OUT=cif; export RDS\_OUT; \

    s2r -v -r sdetm\_b\_l\_scan > s2r.out

\_dreal : sdetm\_b\_l\_scan.cif

    RDS\_TECHNO\_NAME=./techno/techno-035.rds; \

    export RDS\_TECHNO\_NAME; \

    RDS\_IN=cif; export RDS\_IN; \

    dreal -l sdetm\_b\_l\_scan

# .ioc file

LEFT(

(IOPIN scanin.0 );

(IOPIN day\_time.0 );

(IOPIN code(0).0 ); )

TOP(

(IOPIN code(1).0 );

(IOPIN code(2).0 );

(IOPIN code(3).0 ); )

RIGHT(

(IOPIN test.0 );

(IOPIN reset.0 ); )

BOTTOM(

(IOPIN door.0 );

(IOPIN clk.0 );

(IOPIN alarm.0 );

(IOPIN scanout.0 ); )

# Cougar logs

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@ @

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Netlist extractor ... formerly Lynx

Alliance CAD System 5.0 20090901, cougar 1.21

Copyright (c) 1998-2019, ASIM/LIP6/UPMC

Author(s): Ludovic Jacomme and Gregoire Avot

Contributor(s): Picault Stephane

E-mail : alliance-users@asim.lip6.fr

    ---> Parse technological file ./techno/techno-035.rds

         RDS\_LAMBDA = 24

         RDS\_UNIT = 80

         RDS\_PHYSICAL\_GRID = 2

         MBK\_SCALE\_X = 100

    ---> Extract symbolic figure sdetm\_b\_l\_scan

        ---> Translate Mbk -> Rds

        ---> Build windows

        <--- 100

        ---> Rectangles : 1613

        ---> Figure size : ( -116, -116 )

         ( 30616, 30116 )

        ---> Cut transistors

        <--- 0

        ---> Build equis

        <--- 65

        ---> Delete windows

        ---> Build signals

        <--- 65

        ---> Build instances

        <--- 82

        ---> Build transistors

        <--- 0

        ---> Save netlist

    <--- done !

    ---> Total extracted capacitance

    <--- 0.0pF

# LVX logs

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Gate Netlist Comparator

Alliance CAD System 5.0 20090901, lvx 1.4

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\*\*\*\*\* Loading and flattening sdetm\_b\_l\_scan (vst)...

\*\*\*\*\* Loading and flattening sdetm\_b\_l\_scan (al)...

\*\*\*\*\* Compare Terminals .............

\*\*\*\*\* O.K.  (0 sec)

\*\*\*\*\* Compare Instances ..........

\*\*\*\*\* O.K.  (0 sec)

\*\*\*\*\* Compare Connections ..............

\*\*\*\*\* O.K.  (0 sec)

===== Terminals .......... 14

===== Instances .......... 49

===== Connectors ......... 280

\*\*\*\*\* Netlists are Identical. \*\*\*\*\* (0 sec)

# Durc logs

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@@@@@@@ @@@@@ @@@ @@@@ @@ @@@@

Design Rule Checker

Alliance CAD System 5.0 20090901, druc 5.0

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Flatten DRC on: sdetm\_b\_l\_scan

Delete MBK figure : sdetm\_b\_l\_scan

Load Flatten Rules : ./techno/techno-symb.rds

Unify : sdetm\_b\_l\_scan

Create Ring : sdetm\_b\_l\_scan\_rng

Merge Errorfiles:

Merge Error Instances:

instructionCourante : 000 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56

End DRC on: sdetm\_b\_l\_scan

Saving the Error file figure

Done

8249

Some errors have been detected, see file: sdetm\_b\_l\_scan.drc for detailled